Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential: Collector**

 **Mask Ref: JGA**

**APPROVED BY: DK DIE SIZE .018” X .018” DATE: 9/26/22**

**MFG: ALLEGRO/SPRAGUE THICKNESS .008” P/N: 2N2222A**

**DG 10.1.2**

#### Rev B, 7/19/02